DATA PROCESSOR

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Abstract of **JP 8069447 (A)**

PURPOSE: To speed up program execution by making a specific part in a program into a hardware macro by a rewritable element with mapping data when the program is started. CONSTITUTION: A CPU 11, an FPGA 12 which assists the control operation of the CPU 11, a control circuit 13 which controls the writing of mapping data to the FPGA 12, and a main memory 15 are connected to a system bus 10. When the verification of a source program is completed, the part preferably to be made into a hardware macro is analyzed. The specified part is made into the hardware macro matching characteristics of the FPGA 12. Then the block of the specific part made into the hardware macro is divided and mapped corresponding to the circuit scale of the block and FPGA 12 so as to realize the block by the FPGA 12.; Further, the remaining module part to be executed by the CPU 11 is compiled into a load module, which is put together with the mapping data to form one access unit, so that access units are stored as series of object programs in a hard disk device 21.